This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the substrate being rotated during the formation of semiconductor layer, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein the initial compositional variation is caused by the rotation of the substrate during the formation of the semiconductor layer.

2. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein the substrate has a first lattice constant, the semiconductor layer has a second lattice constant, and the first lattice constant differs from the second lattice constant.

3. (Original) The method of claim 1 wherein a first element has a first concentration, a second element has a second concentration, and each of the first and second concentrations is at least 5%.

4. (Original) The method of claim 1 wherein the initial compositional variation varies periodically within the semiconductor layer in a direction perpendicular to a semiconductor layer deposition direction.

5. (Original) The method of claim 4 wherein the compositional variation defines a column within the semiconductor layer, the column having a width and a period.

6. (Original) The method of claim 5 wherein the columnar period is less than approximately 2000 nanometers.

7. (Original) The method of claim 6 wherein the columnar period is less than approximately 1000 nanometers.

8. (Original) The method of claim 5 wherein the semiconductor layer is annealed at an annealing temperature sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter of the columnar period.

9. (Original) The method of claim 5 wherein the semiconductor layer is annealed for a duration sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter of the columnar period.

10. (Original) The method of claim 1 wherein the initial compositional variation varies in a direction parallel to a semiconductor layer deposition direction and defines a superlattice having a periodicity.

11. (Original) The method of claim 10 wherein the superlattice periodicity is less than approximately 100 nanometers.

12. (Original) The method of claim 11 wherein the superlattice periodicity is less than approximately 50 nanometers.

13. (Original) The method of claim 12 wherein the superlattice periodicity is less than approximately 10 nanometers.

14. (Original) The method of claim 10 wherein the semiconductor layer is annealed at an annealing temperature sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter-period of the superlattice.

15. (Original) The method of claim 10 wherein the semiconductor layer is annealed for a duration sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter-period of the superlattice.

16. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein the semiconductor layer is annealed at an annealing temperature greater than the deposition temperature.

17. (Original) The method of claim 16 wherein the annealing temperature is greater than about 800 °C.

18. (Original) The method of claim 17 wherein the annealing temperature is greater than about 1000 °C.

19. (Previously presented) The method of claim 16 wherein the semiconductor layer is annealed at an annealing temperature below a melting point of the semiconductor layer.

20. (Original) The method of claim 19 wherein the annealing temperature is less than about 1270°C.

21. (Original) The method of claim 1 wherein one of the at least two elements comprises silicon.

22. (Original) The method of claim 1 wherein one of the at least two elements comprises germanium.

23. (Original) The method of claim 1, further comprising:

planarizing a top surface of the semiconductor layer.

24. (Original) The method of claim 23 wherein the top surface of the semiconductor layer is planarized before the semiconductor layer is annealed.

25. (Original) The method of claim 23 wherein the top surface of the semiconductor layer is planarized while the semiconductor layer is annealed.

26. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein one of the at least two elements comprises germanium and the top surface of the semiconductor layer is planarized after the semiconductor layer is annealed.

27. (Previously presented) The method of claim 23 wherein planarizing comprises at least one of chemical-mechanical polishing, plasma planarization, wet chemical etching, gas-phase chemical etching, oxidation followed by stripping, and cluster ion beam planarization.

28. (Original) The method of claim 27 wherein chemical-mechanical polishing comprises a first and a second step and the semiconductor layer is annealed between the first and the second chemical-mechanical polishing steps.

29. (Original) The method of claim 27 wherein chemical-mechanical polishing comprises a first and a second step and the semiconductor layer is annealed before the first chemical-mechanical polishing step.

30. (Previously presented) The method of claim 27 wherein ~~planarizating~~ planarizing comprises a high temperature step and the semiconductor layer is annealed during the high temperature planarization step.

31. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer;

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer;

planarizing a top surface of the semiconductor layer;

bonding a top surface of the semiconductor layer to a wafer; and

removing at least a portion of the substrate,

wherein at least a portion of the semiconductor layer remains bonded to the wafer after the portion of the substrate is removed.

32. (Original) The method of claim 23, further comprising:

forming a second layer over the semiconductor layer subsequent to planarizing the top surface of the semiconductor layer.

33. (Original) The method of claim 32 wherein the second layer comprises a material having a lattice constant substantially equal to a lattice constant of the semiconductor layer.

34. (Original) The method of claim 32 wherein the second layer comprises a material having a lattice constant substantially different from a lattice constant of the semiconductor layer.

35. (Previously presented) A method for forming a semiconductor substrate, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements, the elements being distributed to define an initial compositional variation within the semiconductor layer;

annealing the semiconductor layer to reduce the initial compositional variation;

planarizing a top surface of the semiconductor layer;

forming a second layer over the semiconductor layer subsequent to planarizing the top surface of the semiconductor layer;

bonding a top surface of the second layer to a wafer; and

removing at least a portion of the substrate,

wherein at least a portion of the second layer remains bonded to the wafer after the portion of the substrate is removed.

36. (Original) The method of claim 32 wherein the second layer comprises (i) a lower portion having a superlattice and (ii) an upper portion disposed over the lower portion, the upper portion being substantially free of a superlattice.

37. (Original) The method of claim 1 wherein the semiconductor layer has an undulating surface.

38. (Previously presented) The method of claim 37 wherein the undulating surface is formed during deposition of the semiconductor layer.

39. (Original) The method of claim 38 wherein the substrate has an undulating substrate surface and the undulating substrate surface induces the formation of the undulating surface of the semiconductor layer.

40. (Original) The method of claim 37 wherein the undulating surface has an amplitude, the initial compositional variation defines a superlattice having a periodicity, and the periodicity of the superlattice is less than the amplitude of the undulating surface.

41. (Original) The method of claim 1, further comprising:

forming a relaxed graded layer over the substrate,

wherein the semiconductor layer is formed over the relaxed graded layer.

42. (Original) The method of claim 1, further comprising:

forming a protective layer over the semiconductor layer prior to annealing the semiconductor layer.

43. (Original) The method of claim 42 wherein the protective layer comprises a material that is substantially inert with respect to the semiconductor layer.

44. (Original) The method of claim 43 wherein the protective layer is selected from the group consisting of silicon dioxide, silicon nitride, and combinations thereof.

45. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

selecting a first plurality of parameters suitable for forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements, the elements being distributed to define a compositional variation within the semiconductor layer;

forming the semiconductor layer having a haze; and

planarizing the semiconductor layer to remove the haze,

wherein the haze comprises a fine-scale roughness wavelength of <1 micrometer.

46. (Original) The method of claim 45 wherein forming the semiconductor layer comprises forming a lower portion including a superlattice and forming an upper portion over the lower portion, the upper portion being substantially free of a superlattice.

47. (Original) The method of claim 45 wherein the first plurality of parameters comprises at least one parameter selected from the group consisting of temperature, precursor, growth rate, and pressure.

48. (Original) The method of claim 45, further comprising:
cleaning the semiconductor layer after planarizing,
wherein the semiconductor layer remains substantially haze-free after cleaning.

49. (Original) The method of claim 45, further comprising:
selecting a second plurality of parameters suitable for forming a substantially haze-free regrowth layer over the semiconductor layer, the semiconductor layer including at least two elements, the elements being distributed to define a compositional variation within the semiconductor layer; and
forming the substantially haze-free regrowth layer.

50. (Original) The method of claim 49 wherein the first plurality of parameters comprises a first temperature, the second plurality of parameters comprises a second temperature, and the first temperature is higher than the second temperature.

51. (Original) The method of claim 49 wherein the first plurality of parameters comprises a first growth rate, the second plurality of parameters comprises a second growth rate, and the first growth rate is higher than the second growth rate.

52. (Original) The method of claim 49 wherein forming the regrowth layer comprises forming a lower portion including a superlattice and forming an upper portion over the lower portion, the upper portion being substantially free of a superlattice.

53.–75. (Cancelled)

76. (Previously presented) The method of claim 1, wherein the semiconductor layer is formed in a horizontal flow deposition reactor.

77. (Previously presented) The method of claim 1, wherein the rotation of the substrate results in higher fraction of a first element the semiconductor layer disposed in a leading edge of the substrate.

78. (Previously presented) The method of claim 1, wherein the layer is formed in a single wafer reactor.

79. (Previously presented) The method of claim 5, wherein the column comprises a high concentration of a first element, the compositional variation defines a second column within the semiconductor layer, and the second column comprises a low concentration of the first element.

80. (Previously presented) The method of claim 45, wherein after planarization, a top surface of the semiconductor layer has a roughness root-mean-square of less than 5 angstroms in a scan area of 40 $\mu m \times 40$ μm.

81. (Previously presented) The method of claim 80, wherein after planarization, the semiconductor layer top surface has a roughness root-mean-square of less than 1 angstrom in a scan area of 40 $\mu m \times 40$ μm.